Research on Driving and Data Transmission Technology for DMD

Min Qian[1] and Danfeng Hu[2*]

[1]School of Optoelectronic Information Science and Engineering, Soochow University, China
[2]School of Electronics & Information, Soochow University, China

***Corresponding Author:**
Danfeng Hu
No. 1 Shizi Street, School of Electronics & Information,
Soochow University, Suzhou, Jiangsu,
China, 215006.
Email: hdf78@suda.edu.cn

ABSTRACT:
DMD (Digital Micromirror Device) is the core of Digital light processing technology. It is composed of numerous micromirrors' matrix, the frequency of each part can be adjusted. The duration of the lights and darks state was controlled in order to display grayscale images. DMD display hasa lot of advantages, such as low noise, high light efficiency, high resolution, high contrast and long term reliability. In this paper, the driving and data transmission technology using FPGA, combined with DDC4100 driver chip, DAD2000 reset chip and USB chip CY7C68013 were discussed.

Keywords: FPGA, DMD, CY7C68013.

I. INTRODUCTION

DMD is one of the representative products of MEMS[1]. The appearance is shown in Figure 1.It is made of countless micromirrors which is shown in Figure 2. Each micromirror represents a pixel point of the DMD, which is a basic image unit.

Figure 1.Appearance of DMD

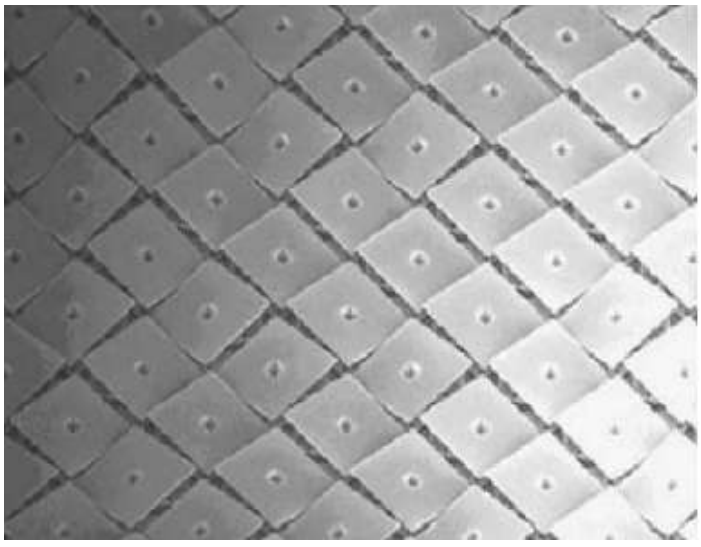

Figure 2.Micromirrors' matrix of DMD

Figure 3 is the expansion diagram of DMD micromirror structure [2]. It mainly consists of CMOS storage function unit, button and frame, reflection lens and three electrodes for offset reduction, mirror addressing and frame addressing.

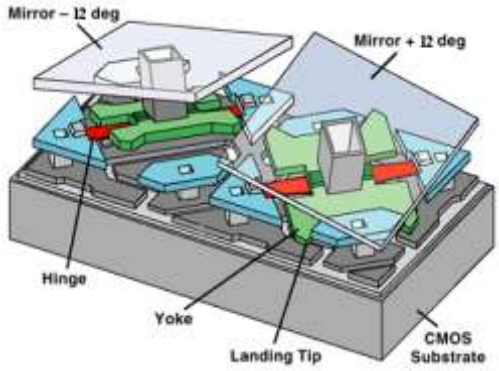

Figure 3. Micromirror structure

Every digital micromirror can be regarded as a miniature optical switch. It will rotate±12°under the control of electrode voltage difference. According to the different rotation angle, the micromirror can be divided into three states: on state, off state and flat state. As shown in Figure 4, on state represents the pixel is light and off state represents the pixel is dark. Before the circuit is power off, all the micromirrors must be set to flat state in order to release the tension. In other words, the DMD relies on switching on and off to display images. When this was controlled by PWM signal, the grayscale images can be displayed.

In this paper, we focus on how to transfer data from the PC to the control circuit by USB and drive DMD to work by FPGA. The hardware and software of this system are introduced.

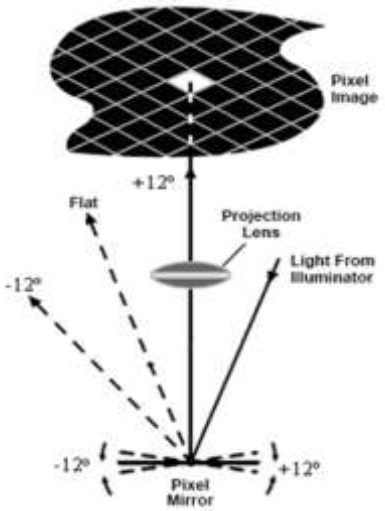

Figure 4.The principle of display images

II. HARDWARE PLATFORM

The hardware platform we used is the TI DLP Discovery 4100. It comprises DDC4100 unit, users' FPGA unit and peripheral circuitetc [3]. The FPGA module is used to process data, transmit data and generate timing control signals, while the DDC4100 module is used to control DMD and DAD2000 chips.

The diagram of this platformis shown in Figure 5.

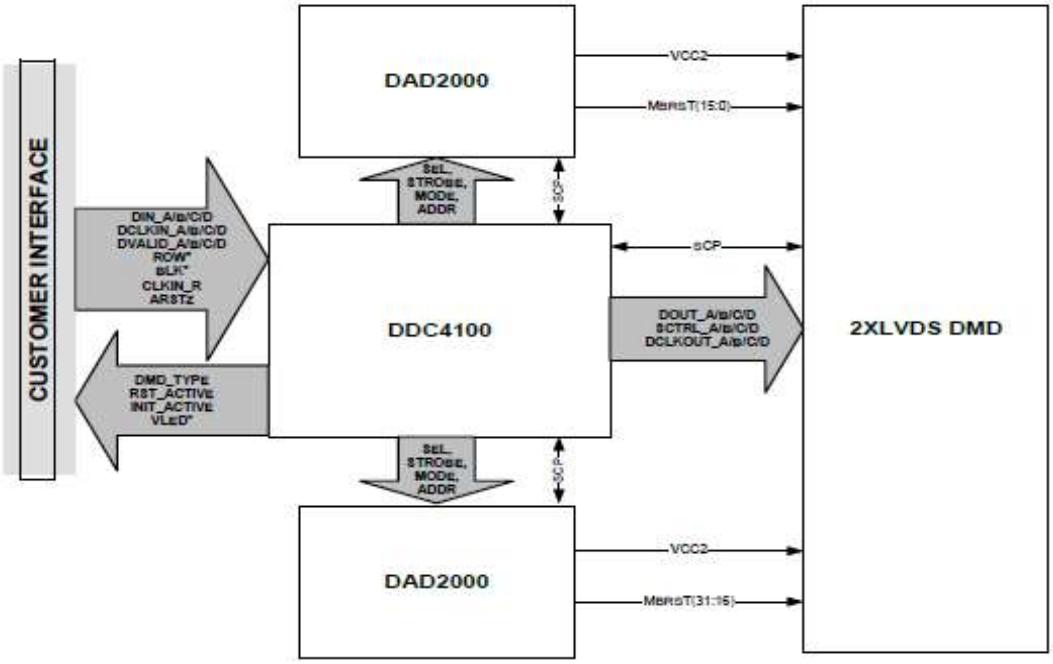

Figure 5. The diagram of hardware platform

The DDC4100 unit converts the data transmitted by the user FPGA through the LVDS bus tothe DMD[4, 5]. In turn, it also sends the DMD information to the FPGA. At the same time, DDC4100 will transmit the control signalsto DAD2000 which control the voltage and reset modesof DMD. It makes the DMD to implement the corresponding flip and realize the image displaying.The user's FPGA in this design belongs to Xilinx VIRTEX5 series[6]. The interface between it and DDC4100 includes DIN, DCLKIN, DVALID, ROW, CLKIN_R, ARSTZ, DMD_TYPE, RST_ACTIVE, INIT_ACTIVE, VLED and other signals.

The function of DAD2000 are controlling the reset process and power supply of DMD. Their outputs are determined by DDC4100. The information between them is transmitted by SEL, STROBE, MODE and ADDR. The DAD2000'sworking voltage is 12V. VBIAS, VRESET and VOFFSET are three output voltage sources. They are outputted in a specific sequence in order to reset DMD.

The USB2.0 controller CY7C68013A is used in this hardware platform[7]. This Single chip integrated USB 2.0 transceiver, smart SIE, and an enhanced 8051 microprocessor. The

logic block diagram is shown in Figure 6.

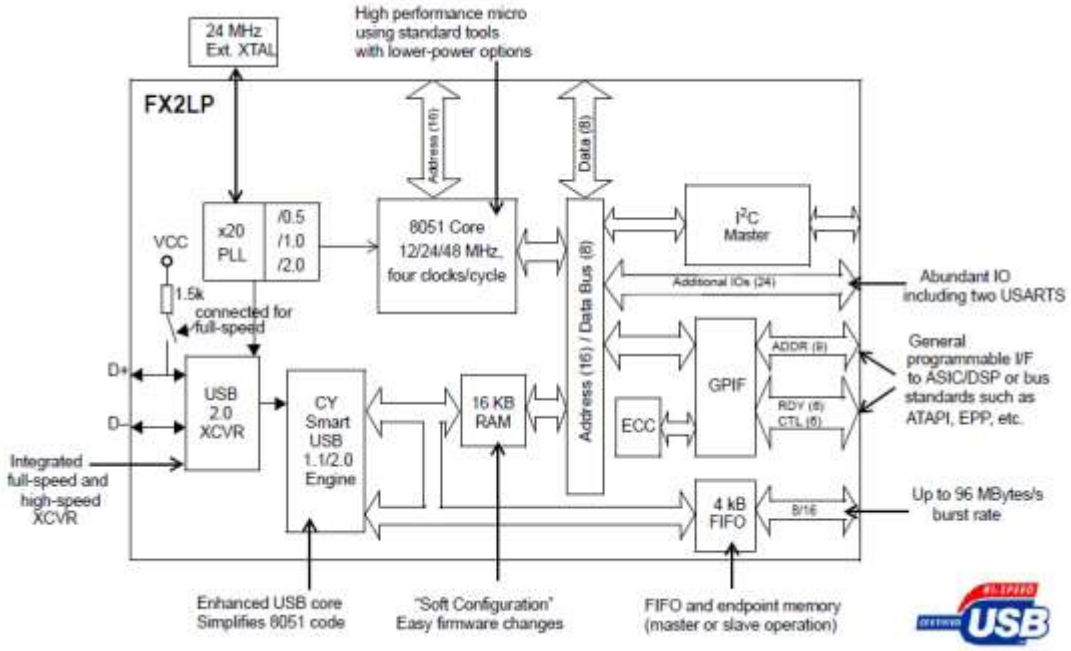

Figure 6. Logic block diagram of CY7C68013A

In this design, CY7C68013A's GPIF interface mode is selected. CY7C68013A gets the data from the computer and transfer them to FPGA through GPIF interface. The data transmission is carried out with the help of external logic circuits. The high-speed communication between FPGA and the computer is realized. The GPIF connections is shown in Figure 7.

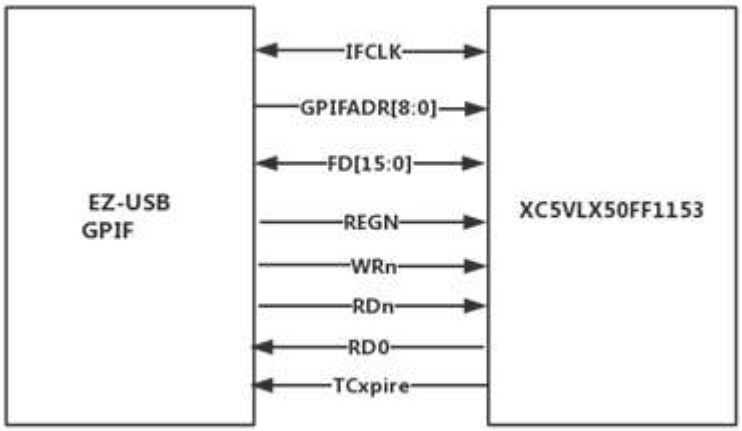

Figure 7. The GPIF connections between FPGA and CY7C68013A

III. FPGA CODE DESIGN

The FPGA code was designed by VHDL and realized in ISE 14.7. The top level module is shown in Figure 8.

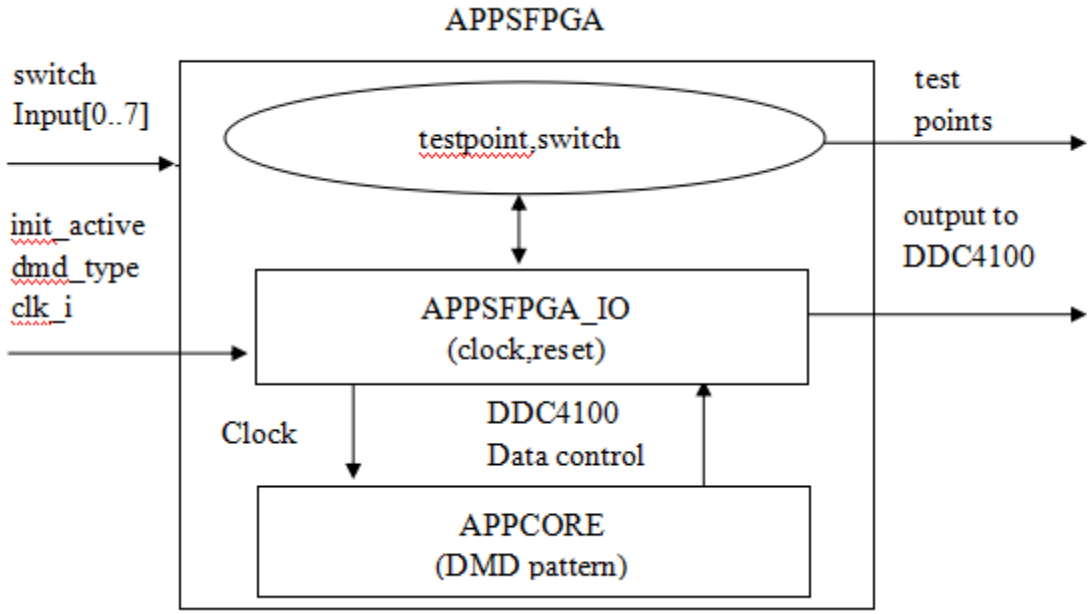

Figure 7. The top level of FPGA code

The APPSFPGA module is mainly divided into two parts. A sub-module is APPSFPGA_IO which realizes clock generating, input signal receiving and differential signal outputting. The other sub modules is APPCORE which generates all kinds of control signals according to the timing diagram of DDC4100.

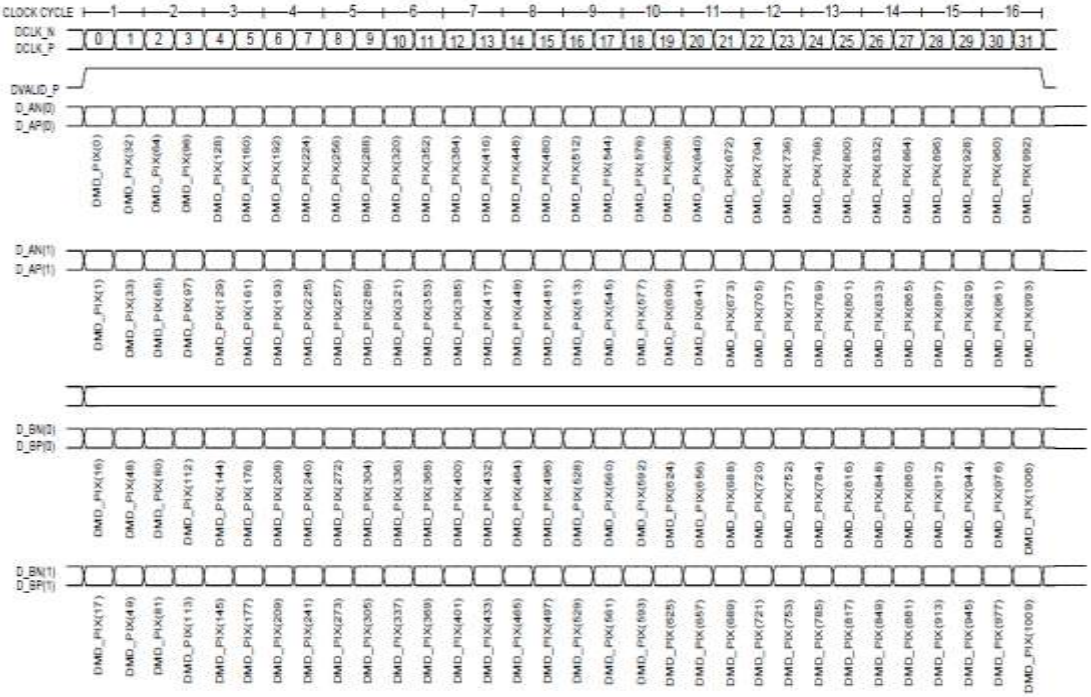

Figure 8. The data timing diagram

Besides the data timing, pgen_rowmd_q, pgen_rowad_q and pgen_blkadare also needed to be set. All this is completed in PGEN file. It is mainly composed of a state machine with several states representing different working procedure. All the state transforming occurs in the system clock rising edge. The state machine diagram is shown in figure 9.

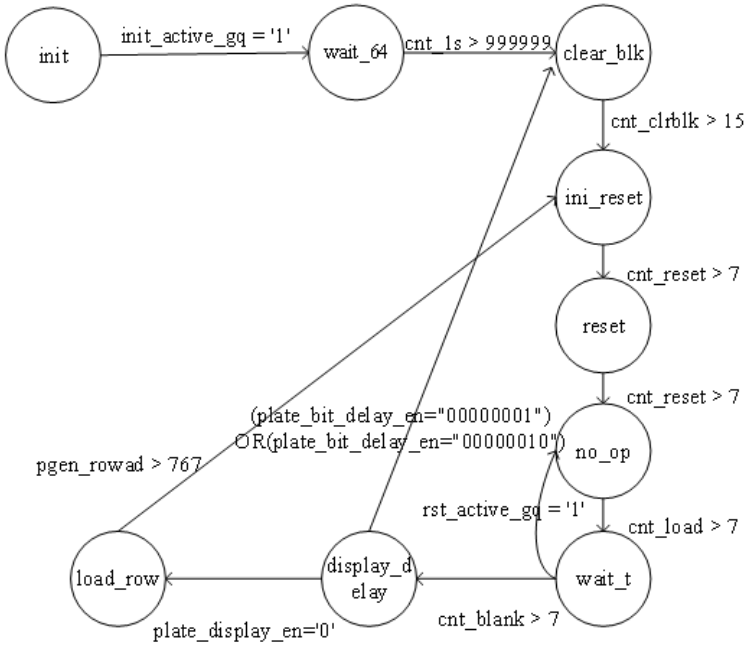

Figure 9. The state machine diagram

IV. USB FIRMWARE DESING

The normal operation of USB devices and the communication tasks require firmware design. The firmware of CY7C68013 runs on the built-in 8051 MCU. It mainly includes the following five contents: initialization, reenumeration, interrupt handling, data receiving and sending, peripheral circuit controlling. Cypress provides some sample codes and firmware framework. Our design is based on these.

CY7C68013 provides seven endpoints: EP0, EP1OUT, EP1IN, EP2, EP4, EP6 and EP8. In this design, endpoint 0 is selected for transmission control, endpoint 2 and endpoint 8 are used for mass data transmission. GPIF mode is selected in this design. It's a host-controlled high-speed data transfer mode. The corresponding interface configuration is realized by the GPIF designer tool, which is shown in figure 10.

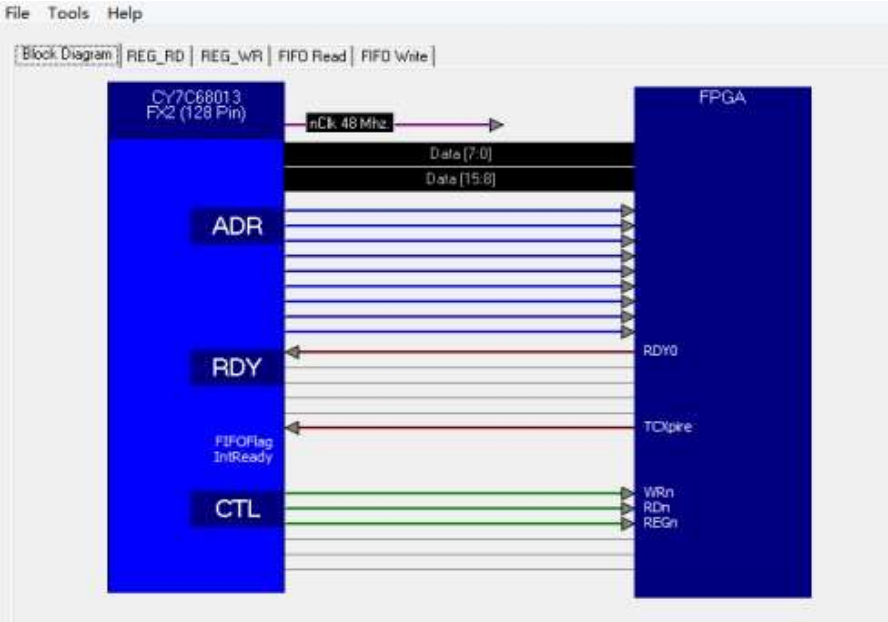

Figure 10. GPIF designer tool

GPIF mode supports loading four waveform descriptors: single-byte writing, single-byte reading, FIFO writing or FIFO reading. Each GPIF waveform descriptor can also be defined as seven working states from S0 to S6. For example, the single-byte reading diagram is shown in Figure 11.

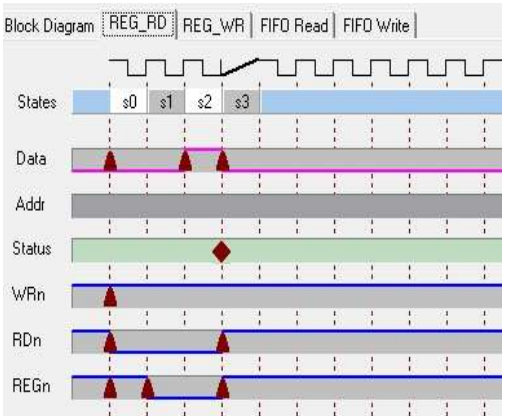

Figure 11. Single-byte reading diagram

For mass data transferring, it is realized by triggering the endpoint directly in the TD_Poll() task scheduling function. Because the EP2 is designed to receive the data from PC, so when the MCU detects the EP2 FIFO is not empty, it will trigger the EP2 data transmission. The part of the code in the TD_Poll() function is shown below.

```
if( GPIFTRIG & 0x80 )
    {
        if ( ! ( EP24FIFOFLGS& 0x02 ) ) //
        {
            SYNCDELAY;
            GPIFTCB1 = EP2FIFOBCH;
            SYNCDELAY;
            GPIFTCB0 = EP2FIFOBCL;
            SYNCDELAY;
            GPIFTRIG = GPIF_EP2;
            SYNCDELAY;
            while( !( GPIFTRIG & 0x80 ) )
            {
                ;
            }
            SYNCDELAY;
        }
    }
```

V. RESULTS

As shown in Figure 12, the grayimage is displayed by DMD. It starts from white, deepens step by step until the final is black.

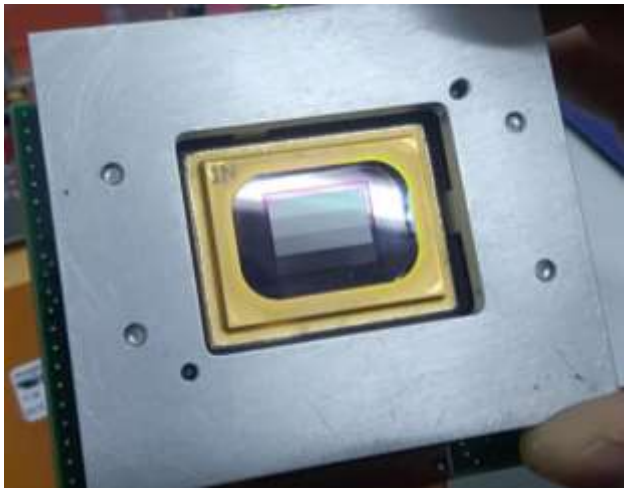

Figure 12. The gray image

A 1024 * 768binary image is transmitted from PC to the FPGA which is shown in Figure 13. Under the control of GPIF mode, it realizes high-speed data transmission.

Figure 13. Data transmission and display

VI. CONCLUSION

In this paper, the DMD driving and data transmission is realized by FPGA coding and USB firmware designing. Some applications will be tested in this platform.

REFERENCES

[1] TEXAS INSTRUMENTS, DLP® Discovery™ 4100 Digital Controller (DDC4100)[S], Data Sheet,TI DN 2510443 Rev C,2011

[2] Texas Instruments. DLP Discovery .7XGA 2x LVDS 12° Type Customer Datasheet [EB/01]. http://www.ti.com/lit/ds/symlink/dlp7000.pdf, June,2013.

[3] TEXAS INSTRUMENTS, DLP® DAD2000 DMD Power and Reset Driver Customer Datasheet[S], TI DN 2506593 Rev G,2011.

[4] S.Ri, M.Fujigaki, Y.Morimoto. DMD Camera and Its Applications to Fringe Pattern Analysis[J]. 2007 SEM Annual Conference,(CD-ROM):1462-1468.

[5] DUDLEY D, DUNCAN W, SLAUGHTER J. Emerging Digital Micromirror Device (DMD) Applications[J]. SPIE,2003,4985:14-25.

[6] Xilinx. Virtex-5 FPGA Data Sheet: DC and Switching Characteristics[EB/01]. http://www.displayalliance.com/storage/1-spec-sheets/XC5VFX100T-2FFG1136C.pdf, May,2010.

[7] Cypress. FX2 Technical Reference Manual Version 2.2[EB/01]. www.cypress.com, 2003.